REMARKS

Applicant thanks the Examiner for the careful review of this application. Claims 1-2, 7-9, 13 and 17 are amended to clarify aspects of the claimed embodiments. New claims 19-23 are introduced for consideration. No new matter was added. Claims 1-23 are currently pending in this application.

REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 1-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over MacInnis (U.S. Patent Application No. 6,738,072). Applicant respectfully traverses.

MacInnis apparently discloses a graphics integrated circuit chip for use in a set-top box for controlling a television display. The graphics chip processes analog video input, digital video input, and graphics input. The chip includes a single polyphase filter that perhaps provides both anti-flutter filtering and scaling of graphics.

Aspects of the claimed embodiments are directed to systems and methods for transmitting a signal containing digital video from stage to stage with little or no jitter. This is accomplished by feeding the digital video into a digital video scaler (DVS) that is connected to a constant-frequency clock. Since the DVS is connected to the constant-frequency clock, the DVS can reclock the frequency of the digital video as it leaves the current stage. Advantageously, jitter is dramatically reduced since the video signal is reclocked to the same frequency as it passes through each stage.

In marked contrast, MacInnis simply does not disclose or suggest for the video signal to be reclocked as it passes through each scaler. Referring to MacInnis' Fig. 2 and related description, it can be seen that MacInnis attempts to correct jitter via a time base corrector (TBC) 72:

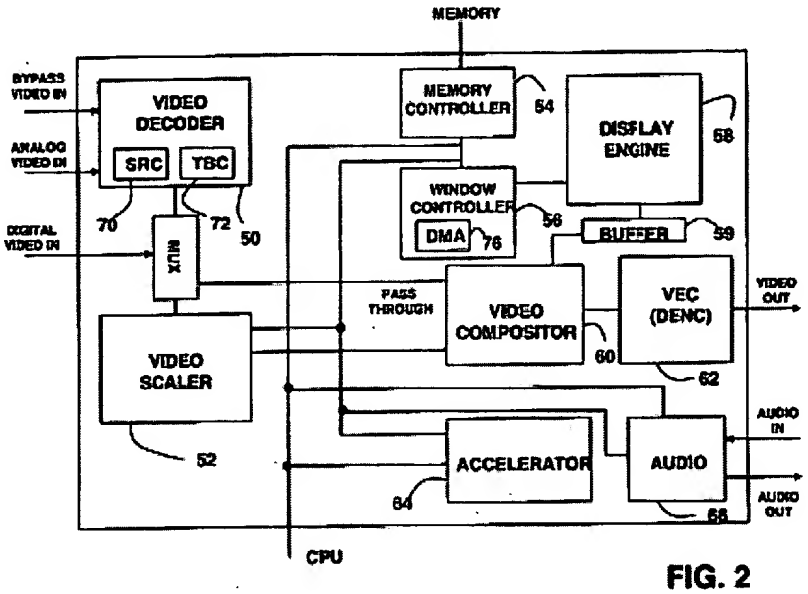


FIG. 2

- MacInnis' Fig. 2

The video decoder (VDEC) **50** preferably digitizes and processes analog input video to produce internal YUV component signals with separated luma and chroma components. In an alternate embodiment, the digitized signals may be processed in another format, such as RGB. The VDEC **50** preferably includes a sample rate converter **70** and a time base corrector **72** that together allow the system to receive non-standard video signals, such as signals from a VCR. The time base corrector **72** enables the video encoder to work in passthrough mode, and corrects digitized analog video in the time domain to reduce or prevent jitter.

-MacInnis, column 4, lines 35-46

As described above, MacInnis' time base corrector 72 is used to reclock a video signal that was converted from an analog video signal and that reclocking

does not take place inside MacInnis' video scaler 52. It should also be further noted that incoming digital video signals, in MacInnis' chip, are not reclocked as they do not pass through the time base corrector 72. Applicant's claimed embodiments simply do not suffer from this deficiency as the video signal is reclocked as it passes through each scaler contained in each stage.

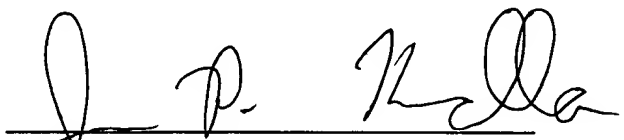
Claims 2-6, 8-12, 14-16 and 18 depend directly or indirectly from independent claims 1, 7, 13 and 17 and are therefore allowable at least for the reasons set forth for these independent claims. Withdrawal of the rejections of claims 1-8 is respectfully requested.

CONCLUSION

Applicant believes that all pending claims are allowable and a Notice of Allowance is respectfully requested. The amendment was made to expedite the prosecution of this application. Applicant respectfully traverses the rejections of the amended claims and reserves the right to re-introduce them and claims of an equivalent scope in a continuation application.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel at the number set out below.

Respectfully submitted,
PERKINS COIE LLP



Dated: September 23, 2005

Jonathan P. Kudla
Reg. No. 47,724

Customer No. 22918
Perkins Coie LLP
P.O. Box 2168
Menlo Park, CA 94026
Telephone: (650) 838-4300